

IMPROVED TOP-OXIDE-EARLY PROCES- SAND ARRAY TOP OXIDE PLANARIZA- TION

Abstract

Manufacturing yield of integrated circuits having differentiated areas such as array and support areas of a memory is improved by reducing height/step height difference between structures in the respective differentiated areas and is particularly effective in conjunction with top-oxide-early (TOE) and top-oxide-late processes. A novel planarization technique avoids damage of active devices, isolation structures and the like due to scratching, chipping or dishing which is particularly effective to improve manufacturing yield using TON processes and also using TOE and TOL processes when average height/step height is substantially equalized. Alternative mask materials such as polysilicon may also be used to simplify and/or improve control of processes.